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## DIAMOND-BASED MICROELECTRONICS

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## Introduction

The need for electronic devices which will reliably operate in the temperature range from 400 to 600°C has made it essential to look beyond conventional electronic materials such as silicon or gallium arsenide. Devices based on these materials are presently able to meet a limited number of elevated temperature demands, but only with the added cost and complexity of an environmental cooling system. Sensors and control devices mounted on or in aircraft engines, operating at temperatures of 500 to 600°C for periods of up to 100 hours, are needed for increased design engineering feedback, and diminished testing and maintenance costs. Integration of the additional weight of the required cooling system for Si devices is already a substantial impediment to increased performance in supersonic aircraft. Electronics to be used in planetary space probes must be capable of extended operation at temperatures above 500°C. Consequently, the environmental cooling system for space based vehicles already accounts for over one-half of current launch vehicle payloads.[1-3] The development of devices intended for operation in high temperature environments would not only meet these existing needs, but would allow many new applications of distributed feedback control.

Due primarily to its wide band gap (5.5 eV) and unequaled thermal conductivity (20 W/cm<sup>2</sup>-K), diamond is being investigated for use in high-temperature devices.[4] Diamond devices already demonstrated at elevated temperatures include diodes, radiation sensors, thermistors, and transistors.[5-9] This paper addresses two fundamental issues in device fabrication, dopant incorporation via ion implantation and ohmic contact formation, and concludes with an evaluation of the device characteristics of an insulated gate FET fabricated using these technologies.

## Dopant Incorporation via Ion Implantation

The ability to form a p-type layer by boron ion implantation is now fairly well established, and claims have been made for the creation of an n-type layer by high temperature lithium implantation. We have utilized a technique based upon that proposed by Prins [10] for boron implantation into type IIA natural diamonds [11,12]. The substrate was a natural semi-insulating (type IIA) diamond with dimensions of 5 mm x 5 mm x 0.25 mm. Boron ions were implanted at 80 K using a multiple implant scheme (25 keV,  $1.5 \times 10^{14}$  B<sup>+</sup>/cm<sup>2</sup>; 50 keV,  $2.1 \times 10^{14}$  B<sup>+</sup>/cm<sup>2</sup>; and 100 keV,  $3.0 \times 10^{14}$  B<sup>+</sup>/cm<sup>2</sup>) intended to provide a uniform p-type layer 210 nm thick. After implantation, the diamond was annealed at 1273 K in nitrogen to remove implantation damage and activate the implanted boron. The carrier concentration and mobility were then determined by making a series of van der Pauw resistivity and Hall effect measure-

ments as a function of temperature. These measurements indicated a room temperature carrier concentration of about  $5 \times 10^{15}$  cm<sup>-3</sup>, with a mobility of about 30 cm<sup>2</sup>/V-s.

## Ohmic Contact Formation

We have investigated the use of Mo, Ti, Ta, and V as ohmic contact metallizations.[13,14] Annealing at high temperature (1223 K) leads to the formation of a carbide layer at the interface, thereby providing an intimate contact with good adhesion to the diamond. A specific contact resistance of  $2 \times 10^{-3}$  Ω-cm<sup>2</sup> was measured for annealed Mo and Ti carbide contacts on highly doped epitaxial films.[15] Specific contact resistance values approximately two orders of magnitude larger have been measured for Mo carbide contacts to lightly doped natural type IIB diamonds. The high temperature stability of the contacts was tested by monitoring the resistance between two contact pads for times of up to 120 hours at 898 K.[16] No change in resistance was observed over time at any given temperature during the experiment. In the case of the non-carbide forming metals Ni, Au, Al, Pd, and Pt [17], however, lack of adhesion is significant, with non-ohmic behavior observed even after annealing at high temperatures.

## Device Fabrication and Testing

We have used the ion implanted layer and refractory metal ohmic contacts to fabricate a demonstration electronic device.[9] The structure chosen was the insulated gate field effect transistor. A circular geometry, consisting of a central drain contact 400 μm in diameter, with concentric 200 μm wide gate and source contacts 1000 μm and 1600 μm in outer diameter respectively, was chosen to eliminate the need for a mesa etch. The source and drain ohmic contacts, consisting of a bilayer structure of 10 nm molybdenum deposited on the diamond with a 160 nm gold cap, were defined using a lift-off process, and then annealed at 1223 K in a hydrogen ambient.

The gate insulator, consisting of an SiO<sub>2</sub> film approximately 100 nm thick, was deposited by indirect plasma enhanced chemical vapor deposition at a temperature of 573 K. The gate metal, also defined by a lift-off process, was a 10 nm titanium/160 nm gold bilayer structure. Titanium was chosen to provide strong adhesion of the gate metallization to the gate insulator. All metallizations were deposited in an ultra-high vacuum system with a pressure during deposition of less than  $7 \times 10^{-8}$  Torr. The devices were then tested in air at temperatures ranging from room temperature to 473 K.

The room temperature transistor characteristics are shown in Figs. 1 and 2. Current saturation and pinch-off are clearly observed. This is the first demonstration of pinch-off in a diamond insulated gate structure. This device may be operated in either the depletion mode (Fig. 1), with a

transconductance of  $28 \mu\text{S mm}^{-1}$ , or in an enhancement mode (Fig. 2), with a transconductance of  $48 \mu\text{S mm}^{-1}$ . (Based on a gate width  $Z$  of  $2\pi(R_{go}-R_{gi})/\ln(R_{go}/R_{gi}) = 2460 \mu\text{m}$ .  $R_{gi}$  and  $R_{go}$  are the inner and outer radii, respectively.) Future performance improvements may be realized by improving the carrier mobility, as discussed in [12]. The source to gate leakage current observed at room temperature was less than  $0.5 \mu\text{A}$ . Device failure above 398 K is attributed to a significant increase observed in this leakage current. A driver-active load circuit utilizing two of these transistors was shown to provide a voltage gain of 2. [17]

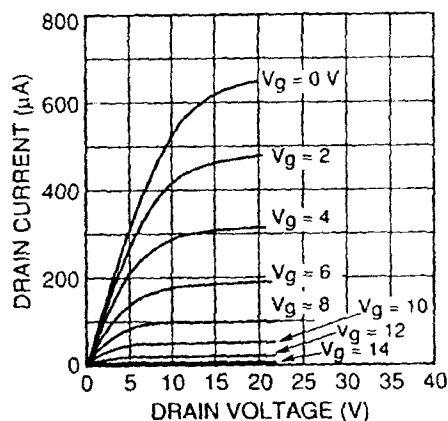


Figure 1. Depletion mode characteristics of the device.

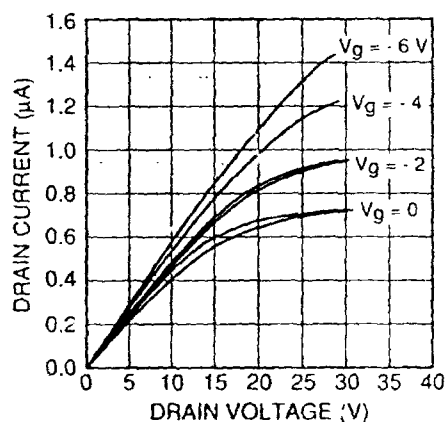


Figure 2. Enhancement mode characteristics of the device.

### Conclusions

Device quality ohmic contacts ( $r_c = 2 \times 10^{-5} \Omega \text{ cm}^2$ ) have been formed to semiconducting diamond. The use of ion implantation to form a conducting layer has been demonstrated, and this conducting layer has been used as the channel layer in a planar IGFET structure exhibiting both current saturation and complete channel pinch-off.

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